EnCore Processor Design Flow

**Synthesis Tools**

- RTL Description
  - Core synthesis/Compiling of macro code definitions and behavioral files.
  - IR to synth: Synthesizes from high-level behavioral descriptions.

- Logic Synthesis
  - Synthesizes complex digital circuits from high-level behavioral descriptions.
  - Verifying the synthesized logic against the original behavioral descriptions.

- Floorplanning
  - Automatically assigns components to specific locations within the chip.
  - RCXplorer: A tool for optimizing the physical layout of the chip.

- Power Analysis
  - Performs power analysis on the design to optimize power consumption.
  - StarXtractor: A tool for extracting power information from the design.

**ASIC Design Flow Steps**

1. **Gate-Level Netlist**
   - Enables the use of automated tools for design and verification.
   - Includes power analysis, timing analysis, and layout extraction.

2. **Timing Analysis**
   - Analyzes the timing of the design to ensure proper operation.
   - Performs comparisons and simulations to validate the design.

3. **Physical Layout**
   - Defines the physical layout of the chip, including power supply and interconnects.
   - Floorplanning: A tool for optimizing the layout of the chip.

**Synthesis Tool Descriptions**

- **RTL Synthesis**
  - Performs behavioral synthesis of high-level design descriptions.
  - Helps in optimizing the design for area, power, and timing.

- **Power Analysis**
  - Evaluates the power consumption of the design.
  - StarXtractor: A tool for extracting power information from the design.

- **Floorplanning**
  - Assigns components to specific locations within the chip.
  - RCXplorer: A tool for optimizing the physical layout of the chip.

**EnCore - Calton Chip Layout**

- **EnCore Processor Design Flow**
  - A flowchart illustrating the design process.
  - Various steps including synthesis, floorplanning, routing, and power analysis.

**Additional Notes**

- **Physical Optimization**
  - Minimizes power consumption and maximizes performance.

- **Floorplanning**
  - Important step in optimizing the layout of the chip.

- **Routing**
  - Ensures that signals can be transmitted efficiently throughout the chip.

- **Power Analysis**
  - Critical for optimizing power consumption and ensuring reliability.

- **EnCore - Calton Chip Layout**
  - Image of the final chip layout.