Quantum 2D Monte Carlo Simulation of MOSFET Transistors using Advanced Architectures

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HPC-Europa2
Pan-European Research Infrastructure on High Performance Computing

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edinburgh data-intensive research

Outline

- The Computer Architecture Group.
- Motivation of the Nanoelectronics Research.
- Parallel 2D Monte Carlo Simulation of Nanoelectronic Devices.
- Assessing the Grid for Nanoelectronics.
- Conclusions.
- Future work: An e-Science Infrastructure for Nanoelectronics.

Introduction of the Computer Architecture Group

Where are we?

Introduction of the Computer Architecture Group

Where are we?

Introduction of the Computer Architecture Group

Research lines

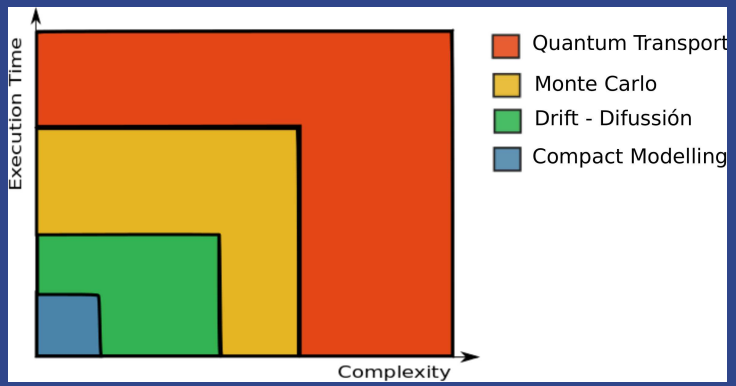
- Signal Processing for Image, Video Coding, and Communications.
- Software and Hardware for Computer Graphics.
- Compilation Techniques for Parallel Computers.
- Computer Arithmetic.
- Memory Hierarchy Optimization in Irregular Problems.
- Run-time Support for Parallelisation and Memory Improvement of Irregular Codes.
- Parallel Simulation of Semiconductor Devices.
- Grid and Cloud Computing.

Introduction of the Computer Architecture Group

Parallel Simulation of Semiconductor Devices

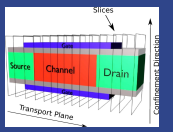
Simulation Techniques

- Drift-Diffusion.
- Monte Carlo.
- NEGF.

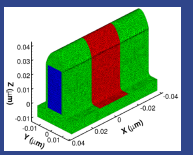


Simulated Devices

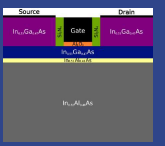
- SOI MOSFETs.



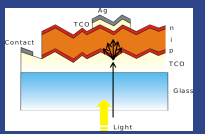
- FinFETs.



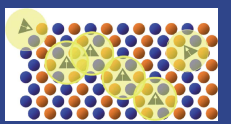
- Heterostructures.



- Solar Cells.



- Spin-Diode.



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Introduction of the Computer Architecture Group

Grid and Cloud Computing

- FORMIGA PROJECT: Integration of computer labs of the university in the es-NGI.
- FORMIGA CLOUD: Development of a Cloud infrastructure using the computer labs of the university.

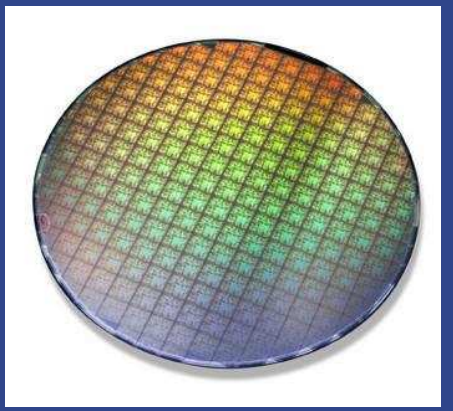
Objectives:

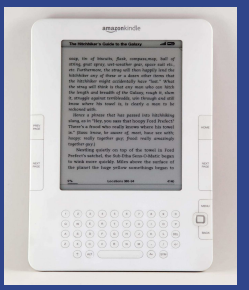
- Increasing the number of available resources for our simulations.
- Learning about new technologies and analysing possible applications.

Motivation of the Nanoelectronics Research

MOSFET Transistor

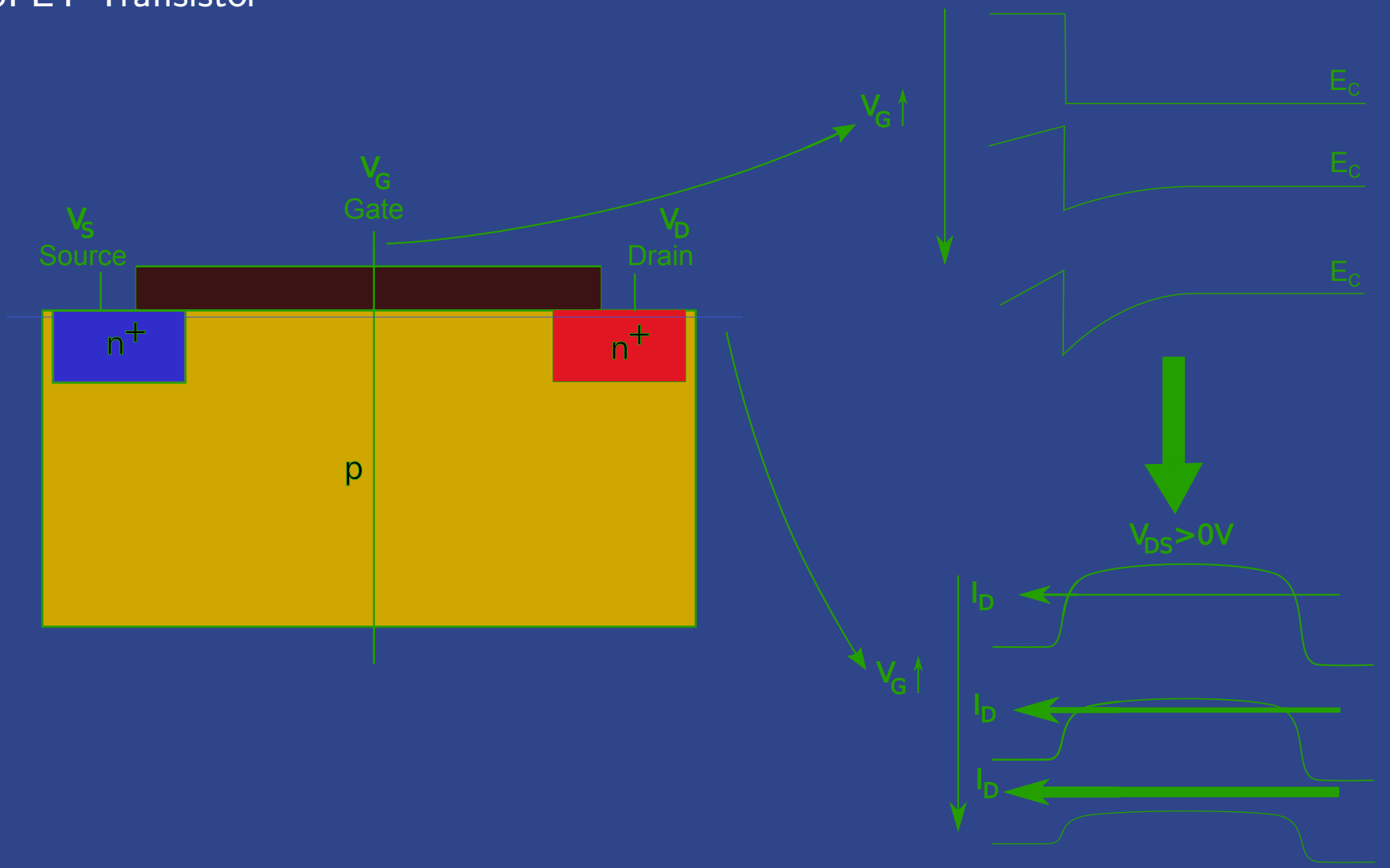
- MOSFET is one of the basic components of the Integrated Circuits now and during the last 50 years.
- Moore's Law: 2x transistors every two years.
- In this period we had an amazing evolution of the electronics.
- Faster processors, mobiles, new electronic devices.





Motivation of the Nanoelectronics Research

MOSFET Transistor



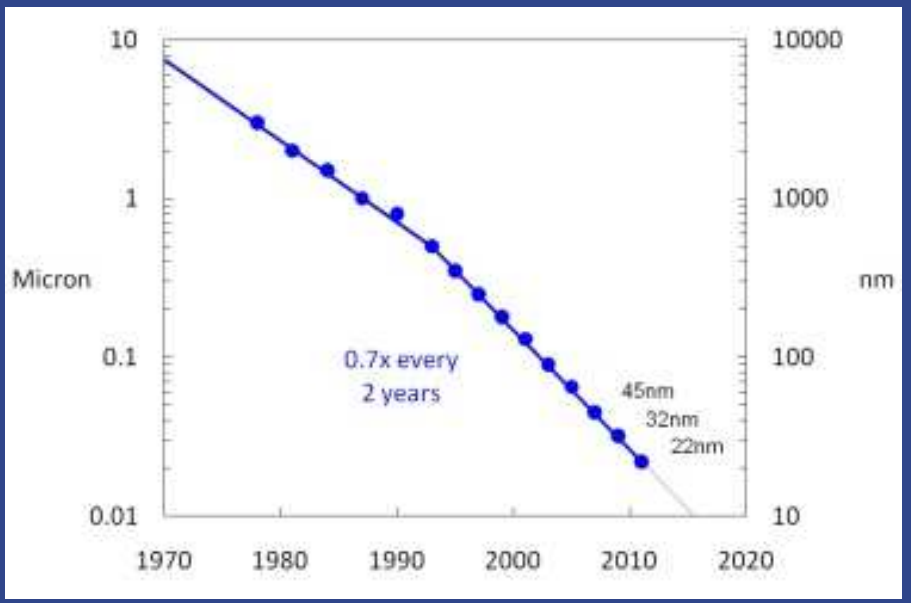
Motivation of the Nanoelectronics Research

End of Traditional Scaling Era

Challenges

- High Speed. 

- Integration. 
- Power Save. 

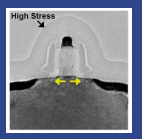


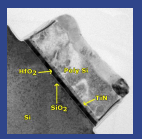
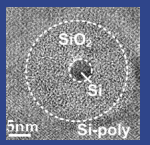
The International Technology Roadmap for Semiconductors (ITRS): Guideline that establishes the challenges on the design of new devices. The 22 nm technological node is the end of the Bulk Technology (ITRS 2010).

Motivation of the Nanoelectronics Research

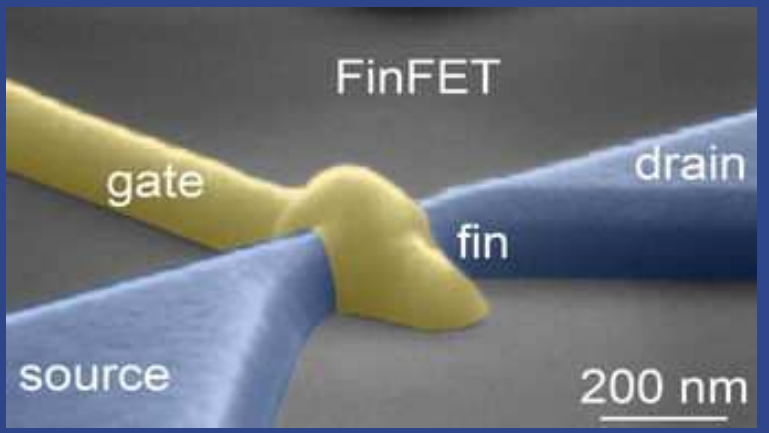
End of Traditional Scaling Era

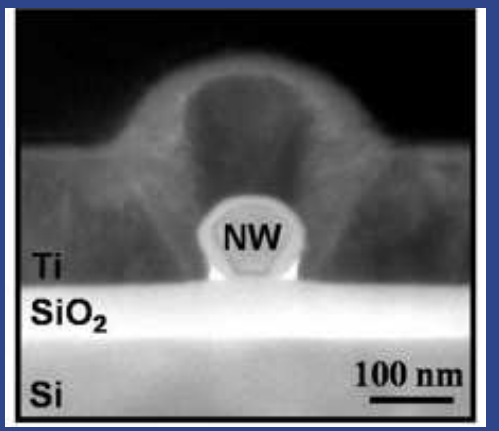
How can Moore's Law continue?

- Strained Silicon. 

- Hi-K. 
- Multigate Devices. 

- SOI Devices. 





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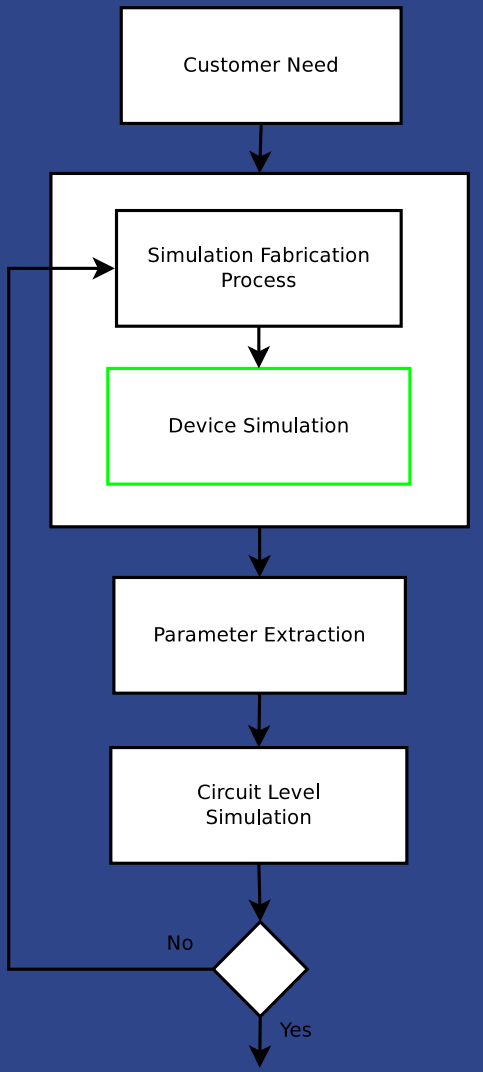
2D Monte Carlo Simulation of Nanoelectronic Devices

Technology for Computer-Aided Design

For technical and economical reasons Technology Computer Aided Design (TCAD) tools complete experimental development techniques.



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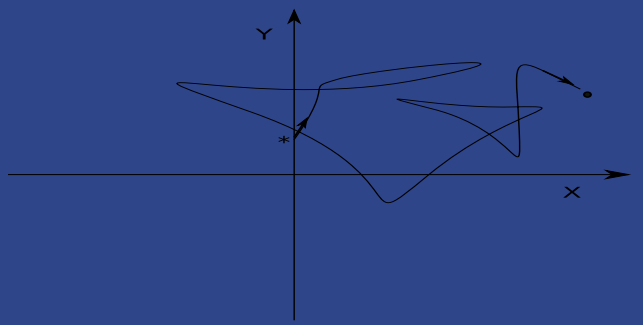
2D Monte Carlo Simulation of Nanoelectronic Devices

Monte Carlo Method

- Numerical method that solves the BTE. Semi-classical transport theory.

$$\partial f/\partial t + \mathbf{v} \cdot \nabla_{\mathbf{r}} f + \dot{\mathbf{k}} \cdot \nabla_{\mathbf{k}} f = \partial f/\partial t|_{coll}$$

- The solution of BTE is obtained from the simulation of the charge carrier transport in the nanoelectronic device.



- Stocastic selection of the flight times and scattering mechanisms.
- SPMC and EMC.

2D Monte Carlo Simulation of Nanoelectronic Devices

OpenMP Parallelisation of 2D MC Simulator

Why do we need parallelism?

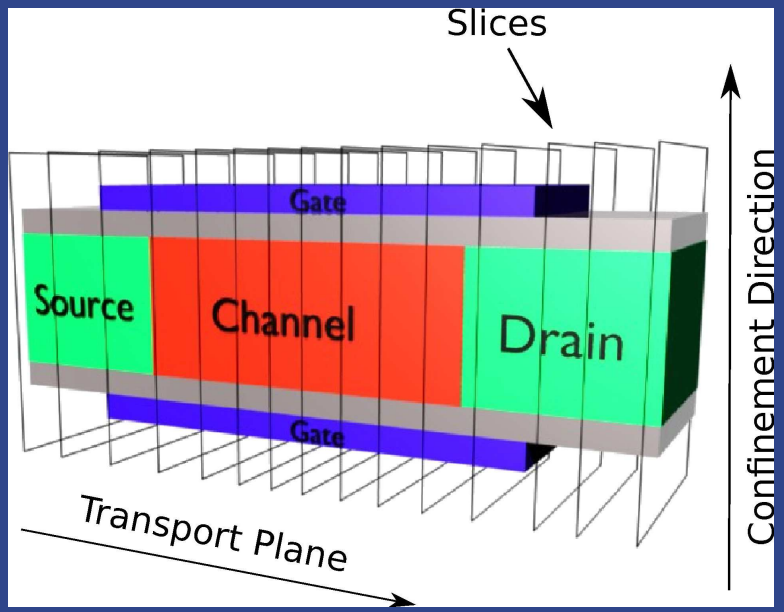
- MC simulators are high demanding computational applications.
- Studying the physical behaviour of a device for 1 ps requires around 1 or 2 hours of computational time.
- Typical simulations are 30 ps length.
- Variability studies requires hundreds or thousands of simulations.

Why OpenMP?

- 92% of the systems of the TOP500 list have multicore processors (November 2010). 73% 4 cores and 19% 6 cores or more.
- De facto standard for shared-memory programming.
- Quite easy programming language.

2D Monte Carlo Simulation of Nanoelectronic Devices

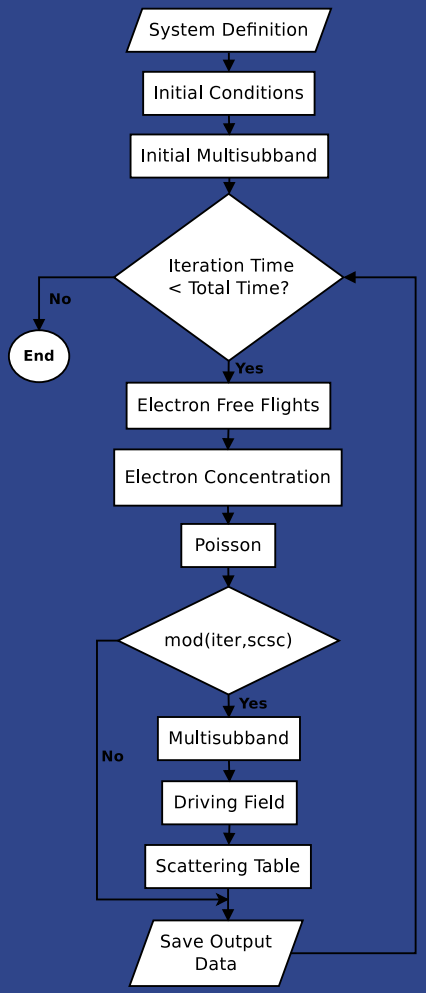
Parallelisation of a 2D Multisubband MC Simulator

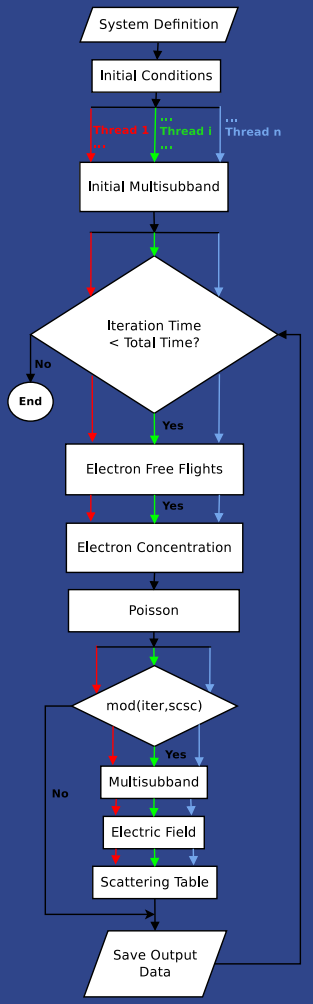


- The 2D Multisubband MC Simulator enables us to simulate the quantum confinement effect on the perpendicular direction to the transport plane.
- BTE is solved in the transport direction.
- Schrödinger equation is solved in the confinement direction.

2D Monte Carlo Simulation of Nanoelectronic Devices

Parallelisation of a 2D Multisubband MC Simulator





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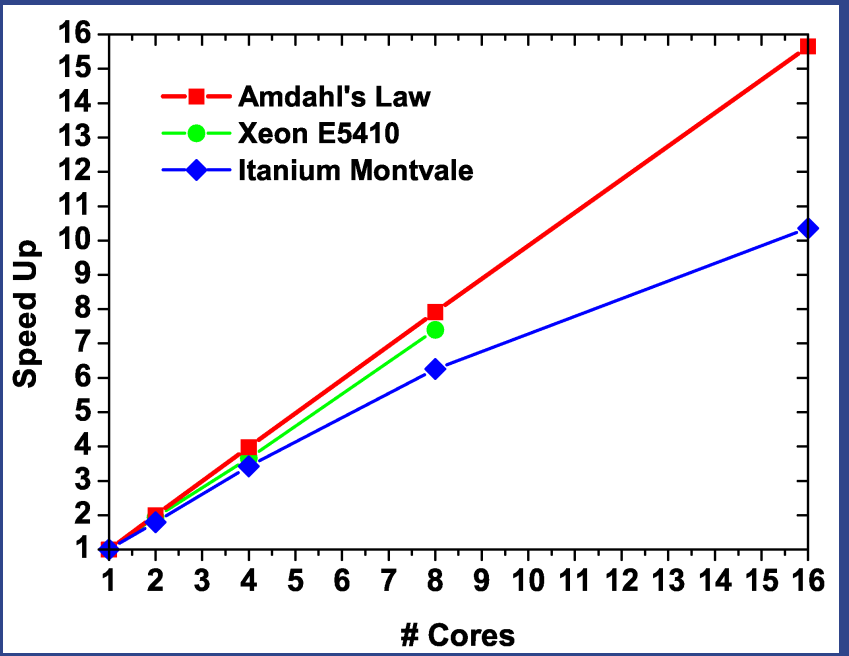
2D Monte Carlo Simulation of Nanoelectronic Devices

Parallelisation of a 2D Multisubband MC Simulator

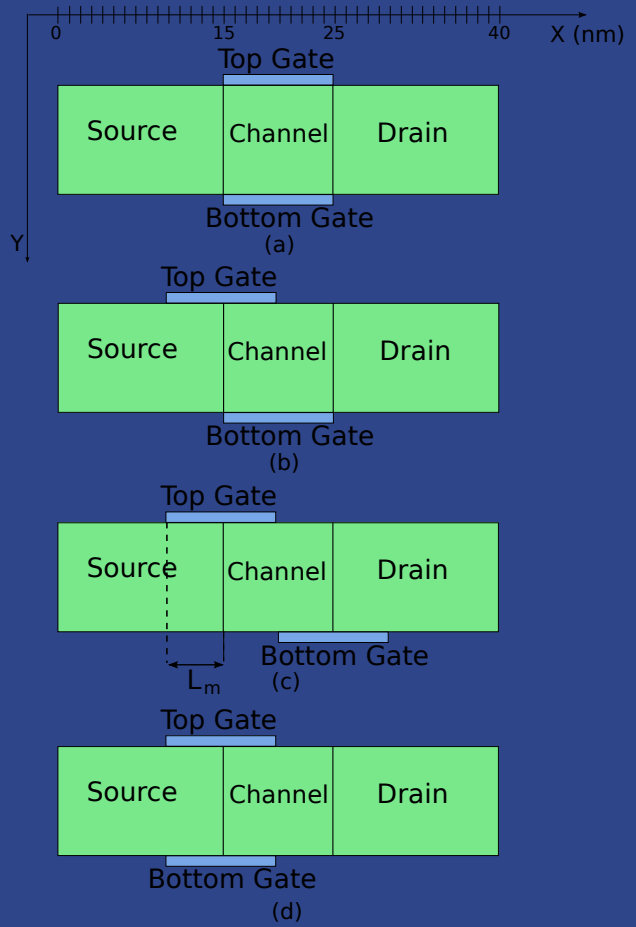
- Execution time has been reduced by a factor 7 with 8 cores.
- We can obtain simulation results faster.
- This allows us to reduce the development time of new models.

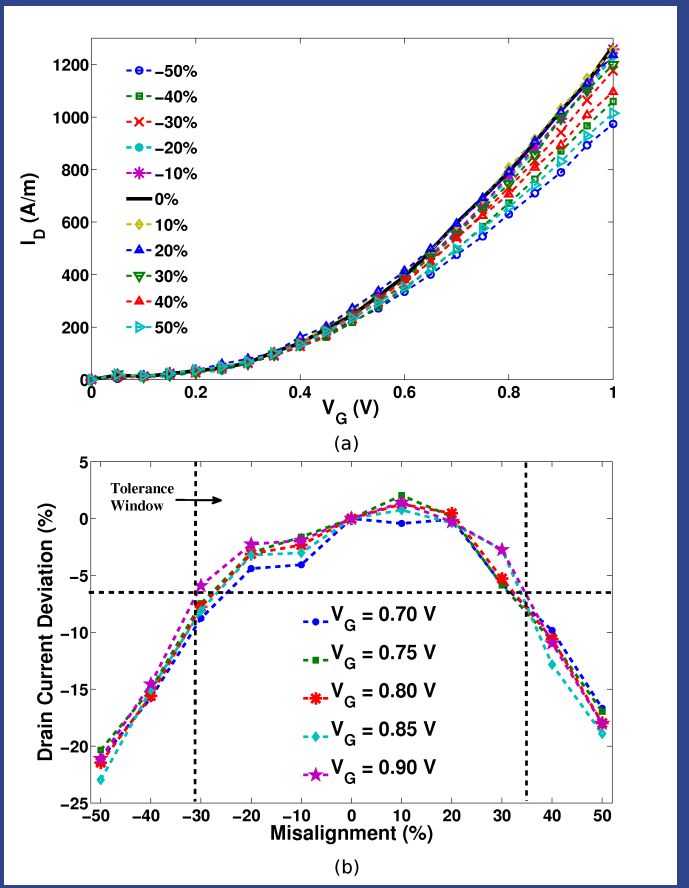


2D Monte Carlo Simulation of Nanoelectronic Devices

Parallelisation of a 2D Multisubband MC Simulator

Studies of parameter variations require a lot of simulations.





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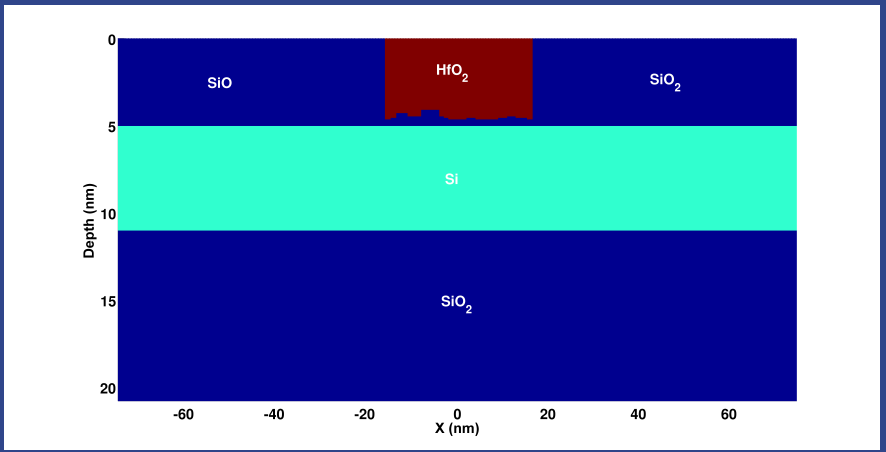
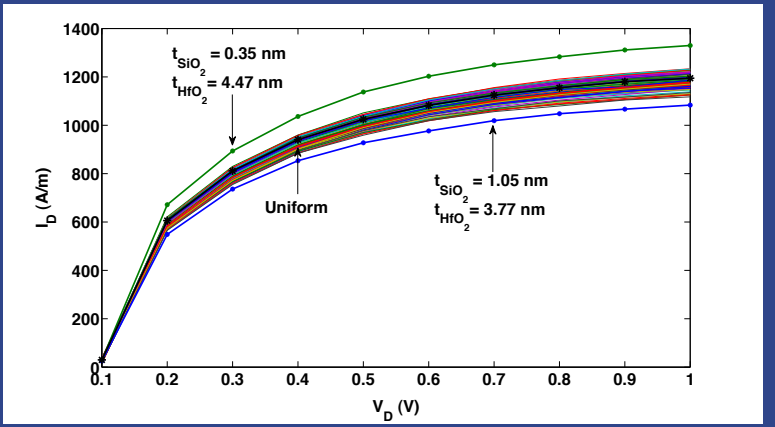
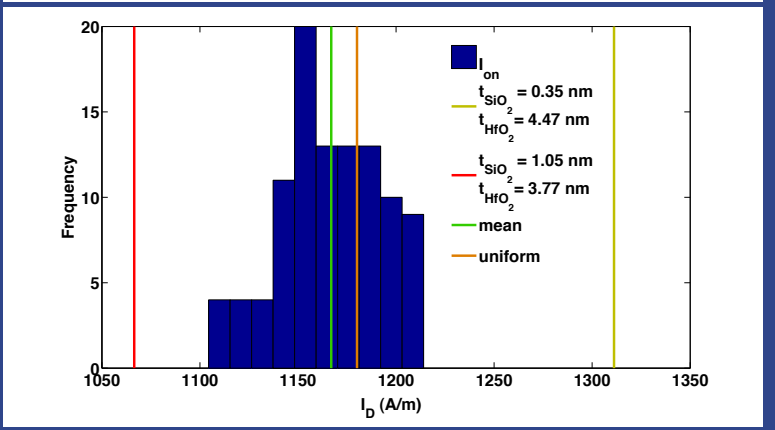
2D Monte Carlo Simulation of Nanoelectronic Devices

Parallelisation of a 2D Multisubband MC Simulator







- Studies of parameter variations require a lot of simulations.
- More resources are necessary. Could be the Grid useful?

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Assessing the Grid

Introduction

- Starting point: FORMIGA PROJECT (2007).
- The creation of the EGI based on NGIs is giving a boost to the NGI development.
- The grid infrastructure of each country will be run by National Grid Initiatives.
- The Spanish NGI (es-NGI) is supported by the Spanish Network for e-Science.

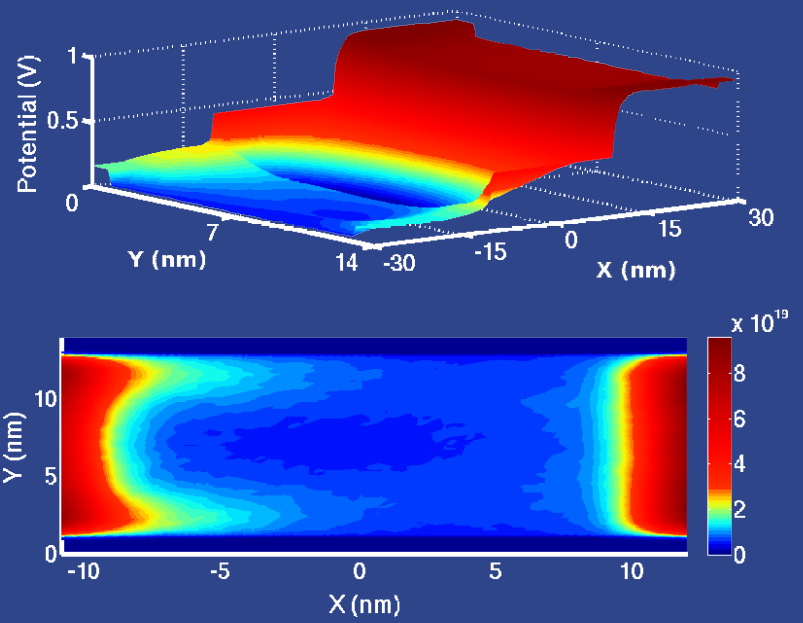
Assessing the Grid

Accessing to the resources

- eng.vo.ibergrid.eu VO belongs to IBERGRID infrastructure.
- It was created in 2010 to support the jobs of the following areas: architecture and, electrical, electronics and automatic engineering.

Initial tasks:

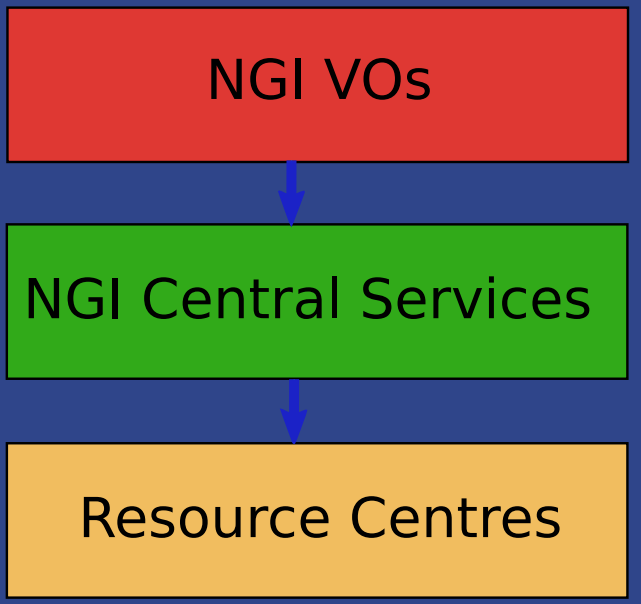
- Assessing the advantages of this infrastructure for nanoelectronics.
- Simplifying the submission and motorization of the jobs.



Assessing the Grid

Services

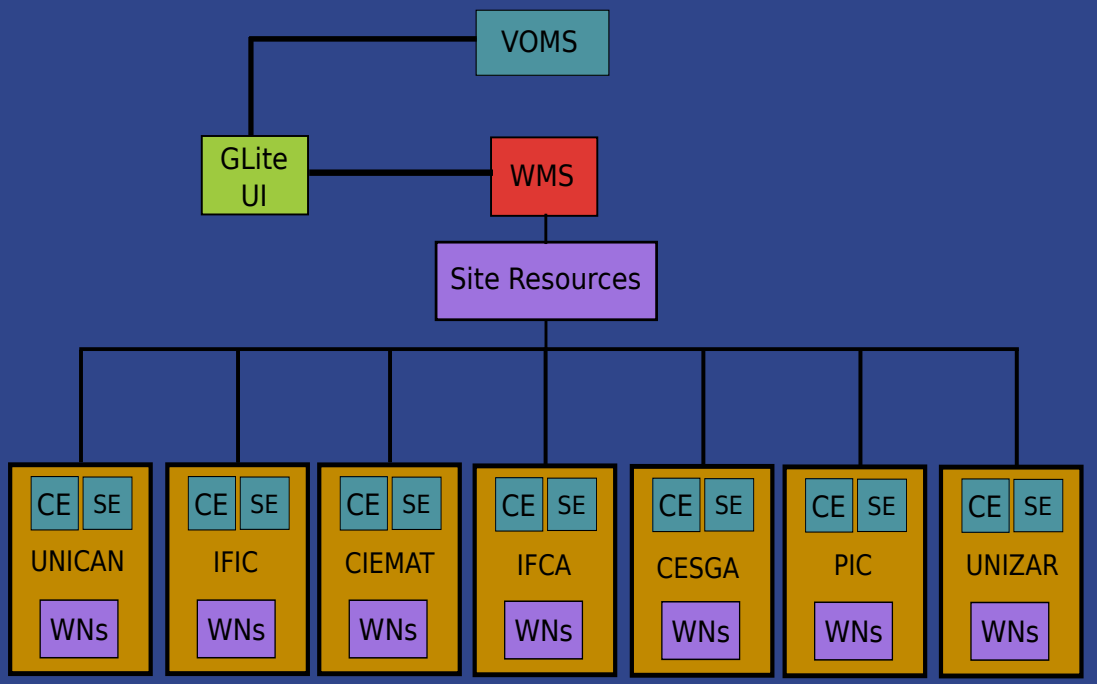
- **Information Service**: provides the state of the resources to the resource broker.
- **Resource Broker**: submits jobs to the resource centres.
- **VOMS**: stores the information about VOs belonging to es-NGI.
- **Storage**: Distributed between the resource centres and available for all VO.
- **File Catalogue**: Localises the stored files.



Moreover, this infrastructure relies on monitoring and accounting services.

Assessing the Grid

Scheme of the VO infrastructure



- Based on GLite middleware.

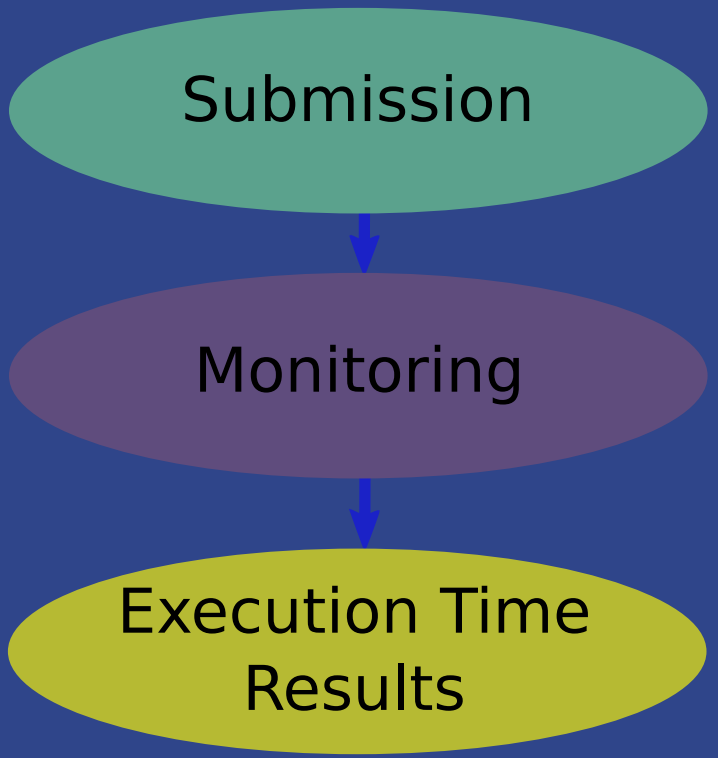
Information obtained from *lcg-infosites* command (2010).

# Cores	Res. Centre
1378	PIC
1616	IFCA
848	IFIC
284	CIEMAT
340	CESGA
148	UNICAN
22	UNIZAR
Total #Cores	4636

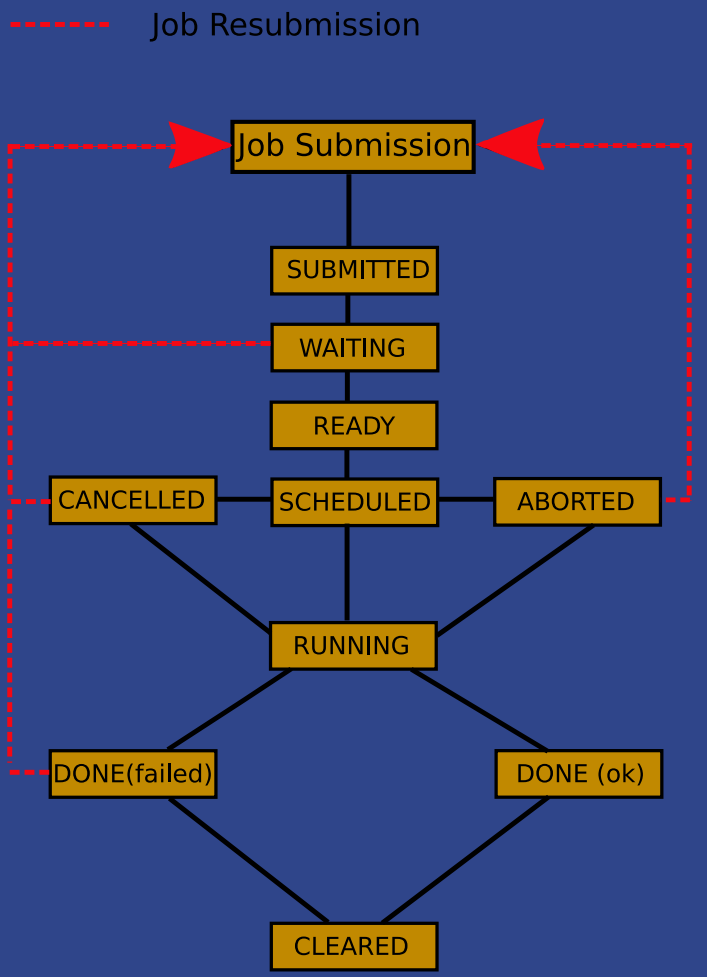
Assessing the Grid

SMNanoS Description

Command line user interface may be a problem for MOSFET VO users. A Python application has been developed to submit and monitor jobs.



Functionality levels.



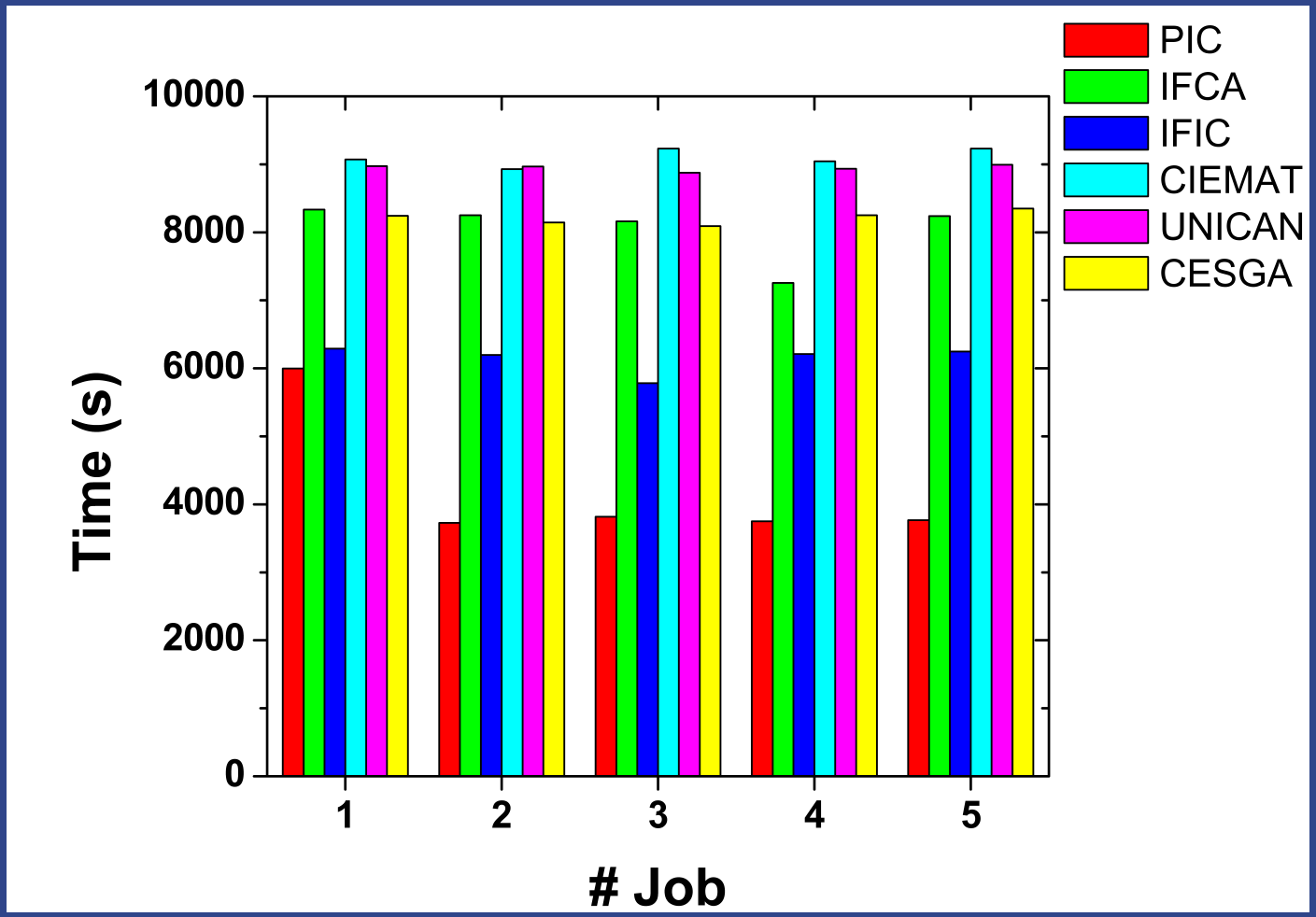
Assessing the Grid

Test Simulation

- We have simulated a job collection with 5 jobs for testing the resource centres.
- Each job simulates a 2 ps length stationary state of a 2D DGSOI MOSFET.
- The execution script of each job saves the execution time, cpuinfo and kernel characteristics of the WN in the SE.
- These simulations were submitted to different resource centres that support our VO.
- Simulation results enable us to evaluate the influence of the resource centres heterogeneity on the execution time.

Assessing the Grid

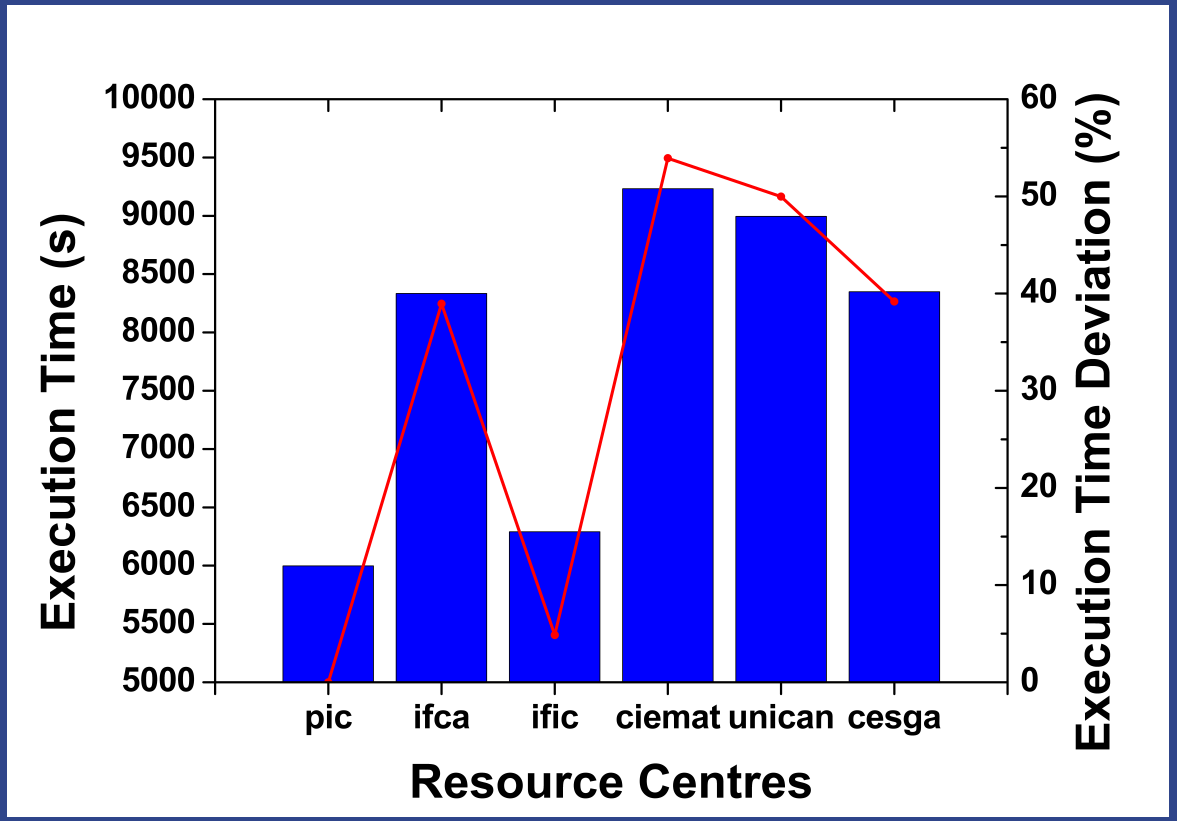
Simulation Results



Execution time of each job of each resource centre.

Assessing the Grid

Simulation Results



Execution time of a job collection = the slowest time of the jobs belonging to the collection. Execution time deviation of the job collections could be over 50%.

Assessing the Grid

Simulation Results

# Res. Centre	CPU	Architecture
PIC	Xeon L5420 2.50 GHz	x86_64
	Xeon L5530 2.40 GHz	x86_64
IFCA	Xeon E5345 2.33 GHz	x86_64
IFIC	Xeon E5420 2.50 GHz	x86_64
CIEMAT	Opteron270 2.0 GHz	i686
UNICAN	PentiumD 3.0 GHz	x86_64
CESGA	Pentium4 3.20 GHz	i686

Processor models of the WNs for each resource centre.

Conclusions

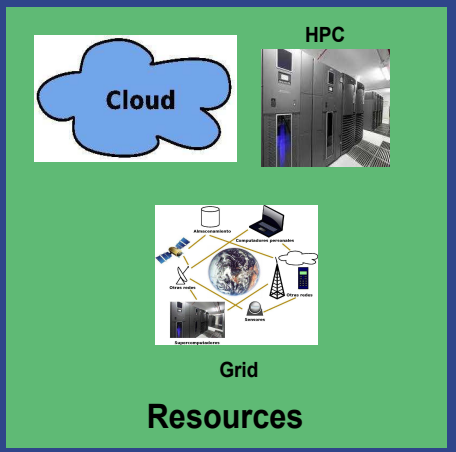
- Scaling of nanoelectronic devices requires new materials and technologies.
- It is necessary to simulate new devices considering advanced physical models.
- Usually, scaled devices require more complex models and therefore, more computational time.
- Parallel simulators enable us to develop new models and get simulation results faster.
- The strong development of multicore processors has encouraged us to adopt OpenMP as the used parallel programming language.
- For example, the parallelisation with OpenMP of a 2D MSB-MC allows us to reduce by 7 the total execution time using 8 cores.

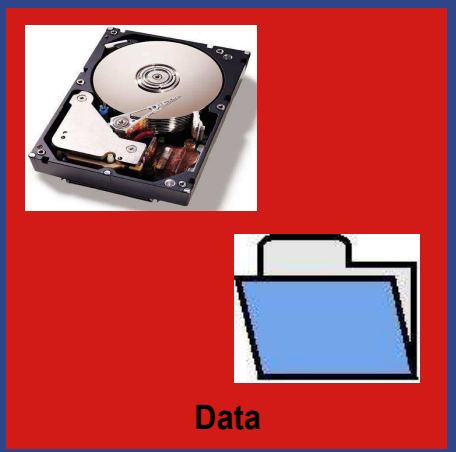
Conclusions

- Thanks to the parallel simulators we can get the results of parameter variations faster. However, more available resources are required.
- Grid infrastructures could be a good option to increase the number of available resources. But several drawbacks have to be overcome:
  - Heterogeneous resources produce until a 50% difference on the execution time of the simulations.
  - Easier technologies for the final users are required. Authentication, submission and monitoring services use archaic command line systems.

Future work: An e-Science Infrastructure for Nanoelectronics

Tidying up the nanoelectronic simulations



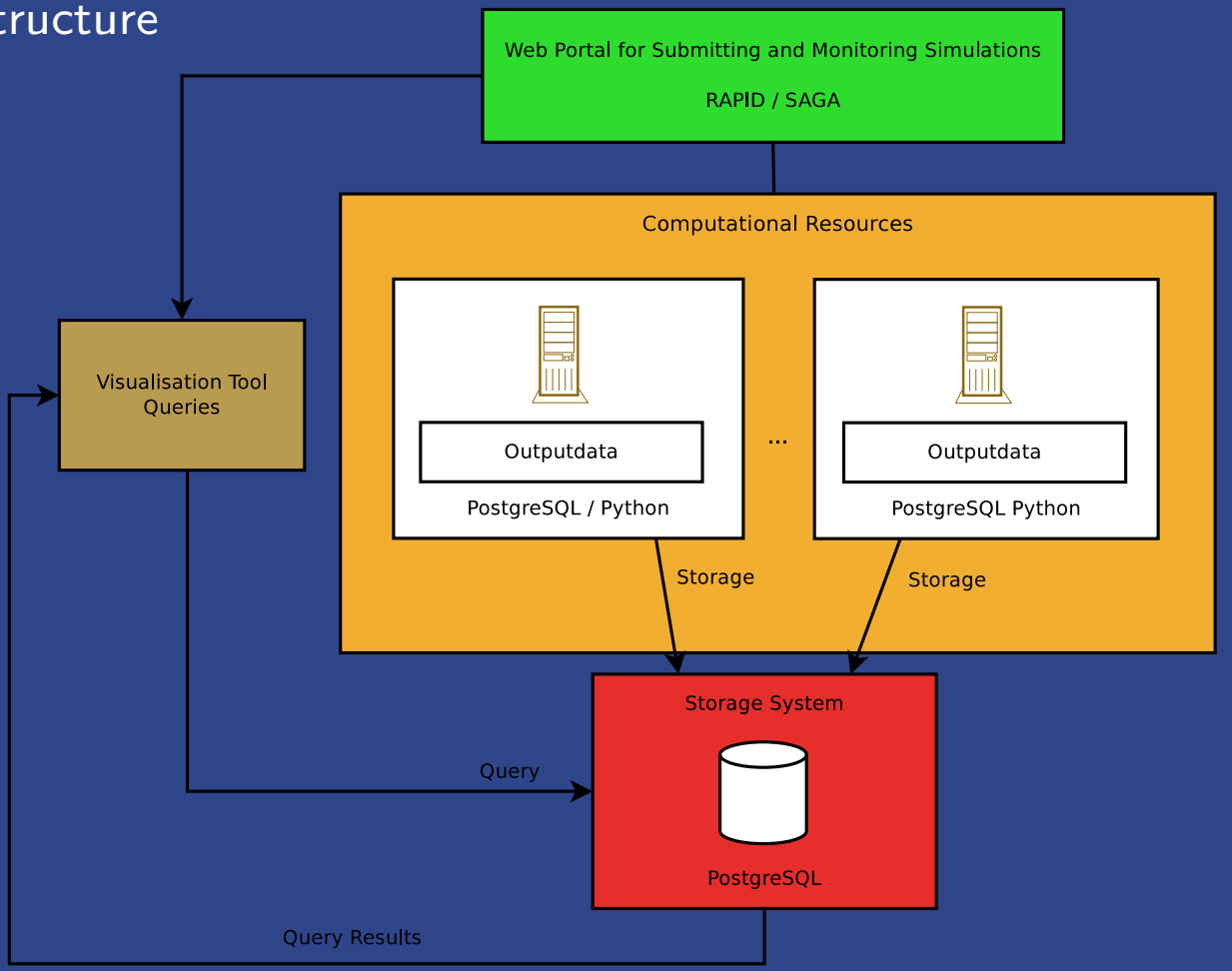


Nanoelectronics requires:

- Access to different infrastructures.
- Run different simulators made with different programming languages.
- Data management systems.
- Visualisation tools.

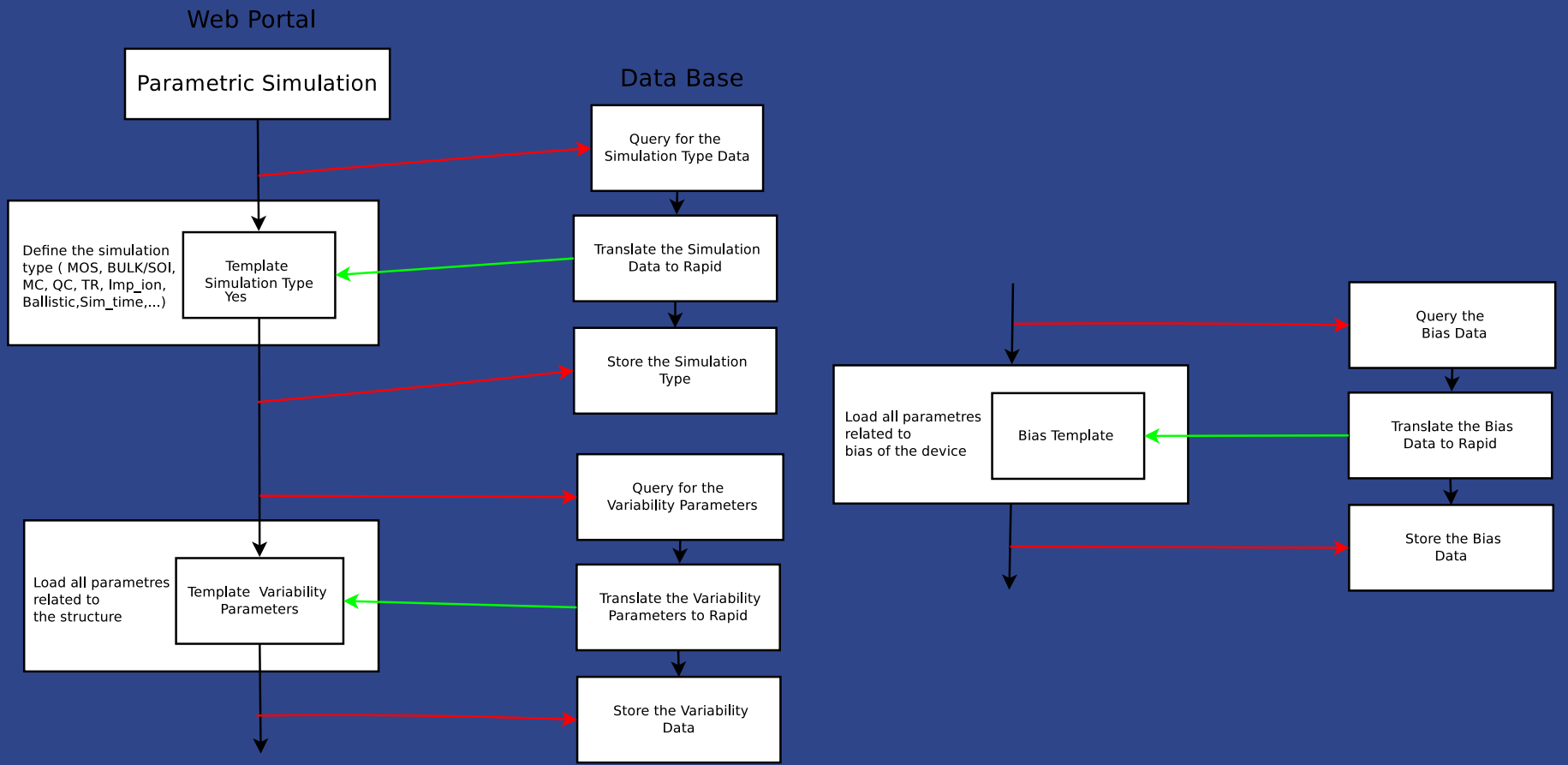
Future work: An e-Science Infrastructure for Nanoelectronics

Proposed Infrastructure



Useful for other research fields. Bioinformatics, Chemistry, etc.

Future work: An e-Science Infrastructure for Nanoelectronics



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Thank you for your attention!

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