EnCore Processor Design Flow
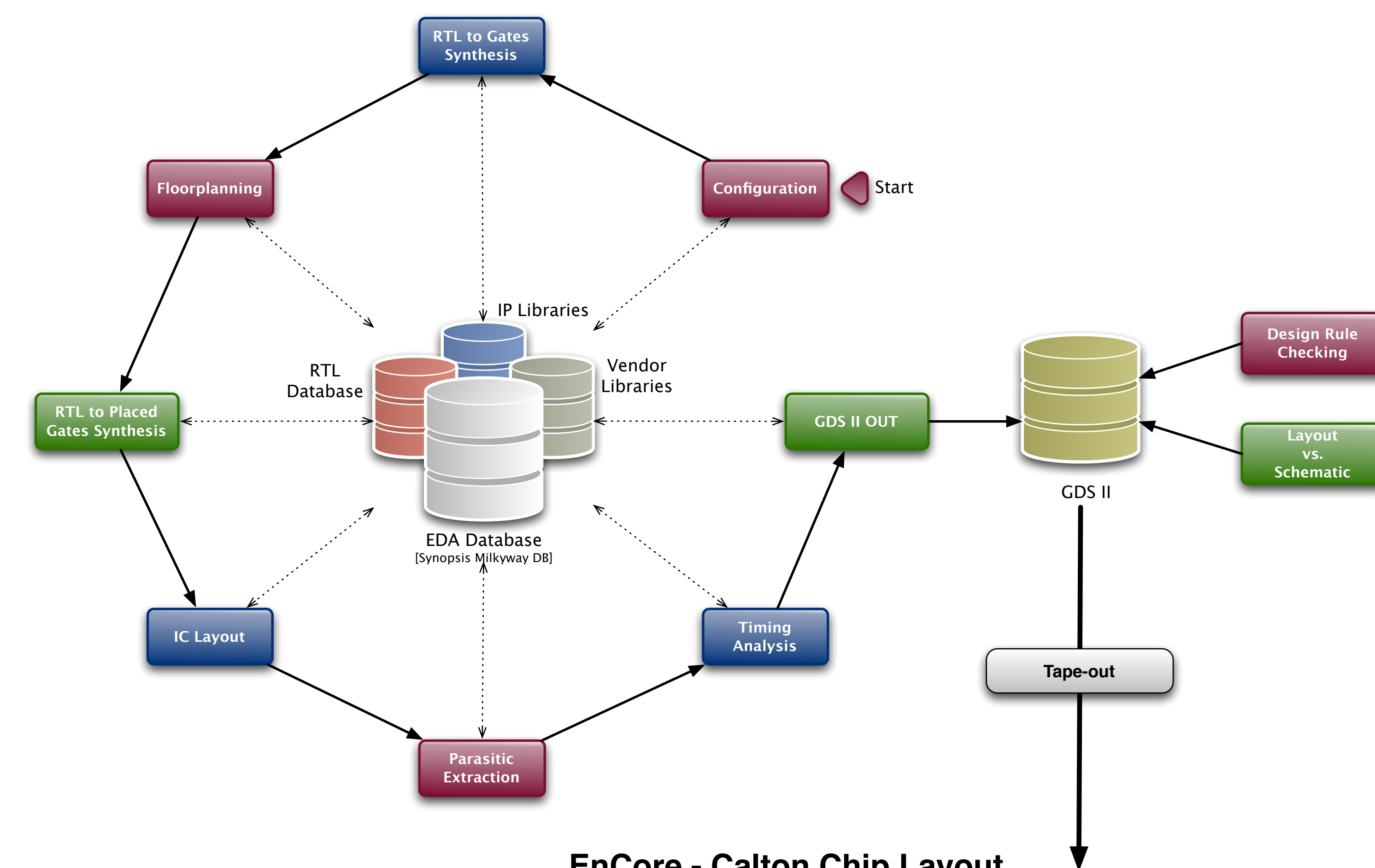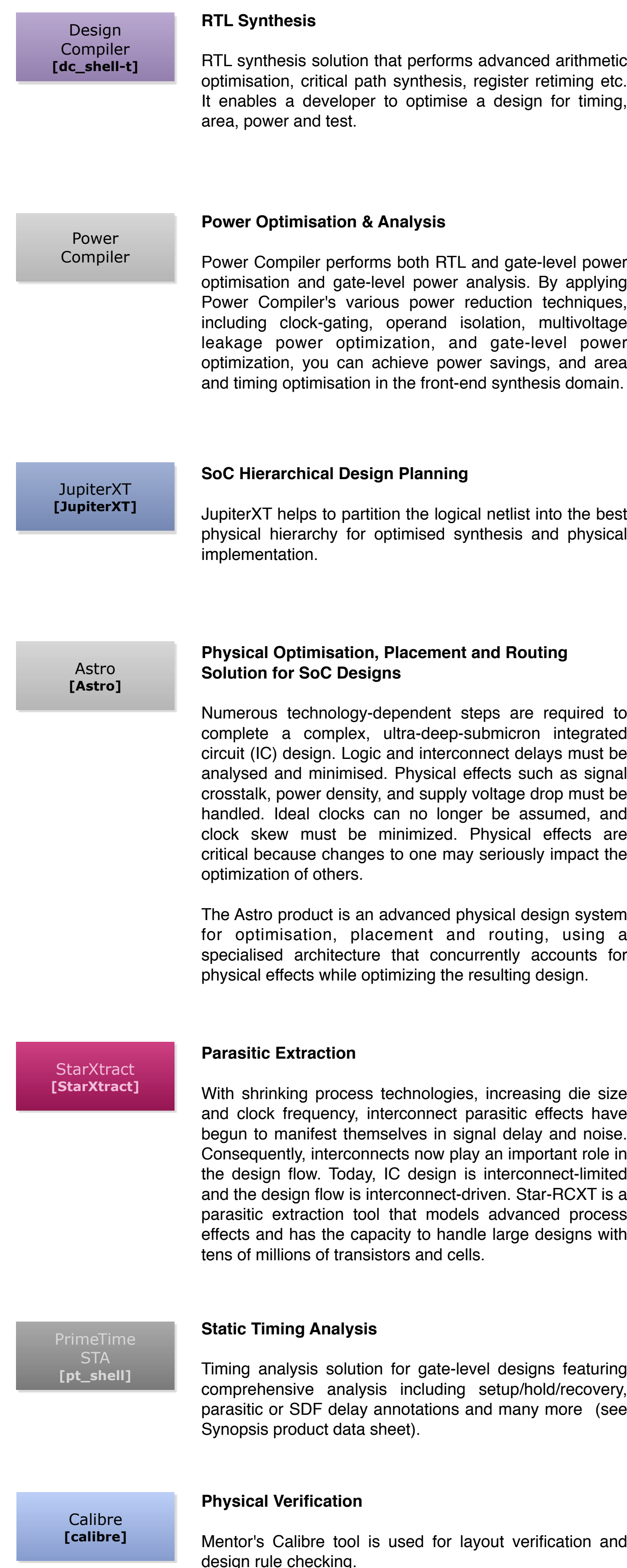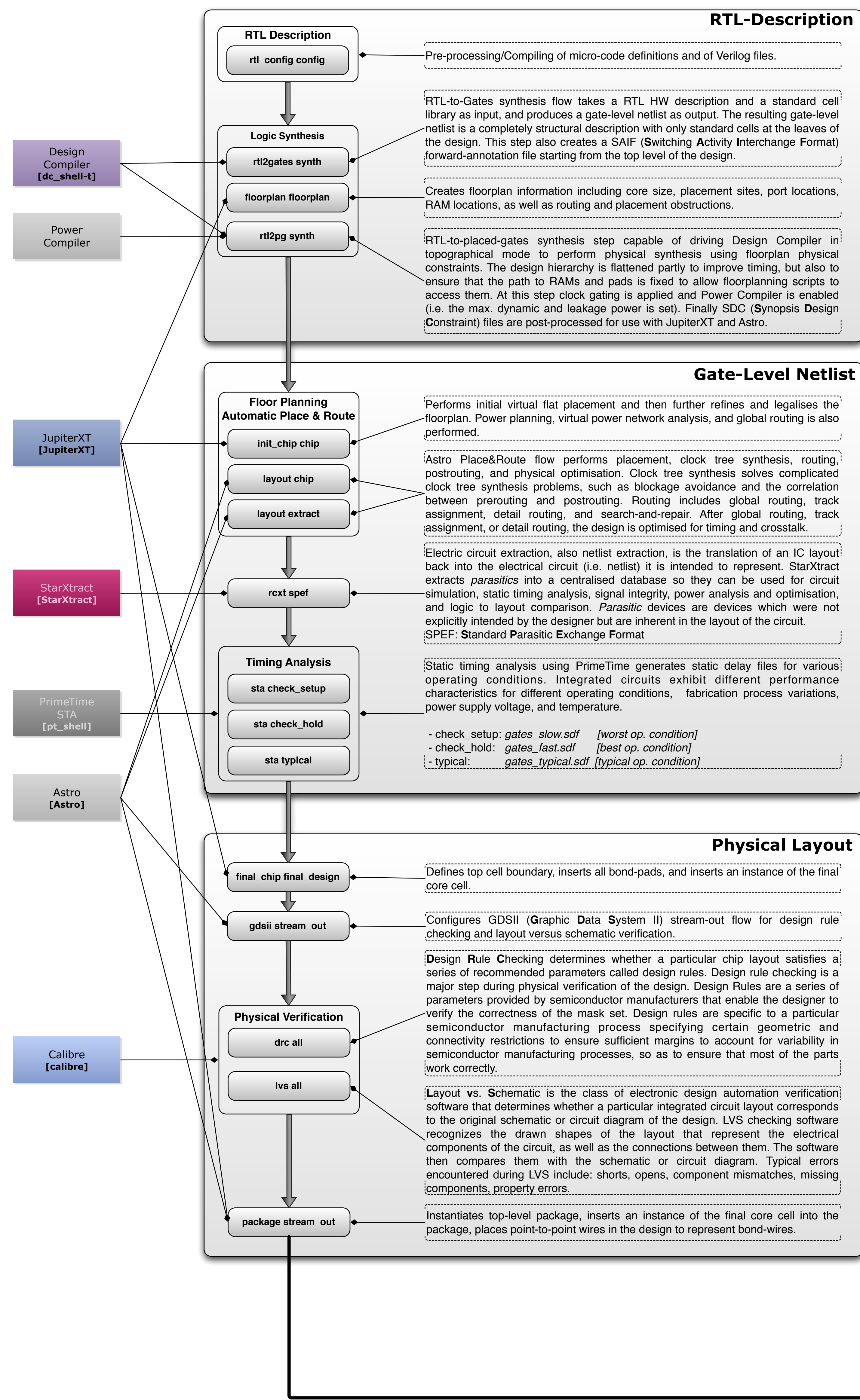
Synthesis Tools

ASIC Design Flow Steps [Makefile targets]

Synthesis Tool Descriptions

RTL-Description

RTL Description
- rtl_config config

Pre-processing/Compiling of micro-code definitions and of Verilog files.

Design Compiler [dc_shell-t]

Logic Synthesis
- rtl2gates synth

RTL-to-Gates synthesis flow takes a RTL HW description and a standard cell library as input, and produces a gate-level netlist as output. The resulting gate-level netlist is a completely structural description with only standard cells at the leaves of the design. This step also creates a SAIF (Switching Activity Interchange Format) forward-annotation file starting from the top level of the design.

Power Compiler

- floorplan floorplan

Creates floorplan information including core size, placement sites, port locations, RAM locations, as well as routing and placement obstructions.

- rtl2pg synth

RTL-to-placed-gates synthesis step capable of driving Design Compiler in topographical mode to perform physical synthesis using floorplan physical constraints. The design hierarchy is flattened partly to improve timing, but also to ensure that the path to RAMs and pads is fixed to allow floorplanning scripts to access them. At this step clock gating is applied and Power Compiler is enabled (i.e. the max. dynamic and leakage power is set). Finally SDC (Synopsis Design Constraint) files are post-processed for use with JupiterXT and Astro.

Gate-Level Netlist

Floor Planning Automatic Place & Route
- init_chip chip

Performs initial virtual flat placement and then further refines and legalises the floorplan. Power planning, virtual power network analysis, and global routing is also performed.

- layout chip

Astro Place&Route flow performs placement, clock tree synthesis, routing, postrouting, and physical optimisation. Clock tree synthesis solves complicated clock tree synthesis problems, such as blockage avoidance and the correlation between prerouting and postrouting. Routing includes global routing, track assignment, detail routing, and search-and-repair. After global routing, track assignment, or detail routing, the design is optimised for timing and crosstalk.

- layout extract

- rcxt spef

Electric circuit extraction, also netlist extraction, is the translation of an IC layout back into the electrical circuit (i.e. netlist) it is intended to represent. StarXtract extracts parasitics into a centralised database so they can be used for circuit simulation, static timing analysis, signal integrity, power analysis and optimisation, and logic to layout comparison. Parasitic devices are devices which were not explicitly intended by the designer but are inherent in the layout of the circuit. SPEF: Standard Parasitic Exchange Format

JupiterXT [JupiterXT]

StarXtract [StarXtract]

Timing Analysis
- sta check_setup
- sta check_hold
- sta typical

Static timing analysis using PrimeTime generates static delay files for various operating conditions. Integrated circuits exhibit different performance characteristics for different operating conditions, fabrication process variations, power supply voltage, and temperature.

- check_setup: gates_slow.sdf   [worst op. condition]
- check_hold: gates_fast.sdf   [best op. condition]
- typical: gates_typical.sdf [typical op. condition]

PrimeTime STA [pt_shell]

Astro [Astro]

Physical Layout

- final_chip final_design

Defines top cell boundary, inserts all bond-pads, and inserts an instance of the final core cell.

- gdsii stream_out

Configures GDSII (Graphic Data System II) stream-out flow for design rule checking and layout versus schematic verification.

Design Rule Checking determines whether a particular chip layout satisfies a series of recommended parameters called design rules. Design rule checking is a major step during physical verification of the design. Design Rules are a series of parameters provided by semiconductor manufacturers that enable the designer to verify the correctness of the mask set. Design rules are specific to a particular semiconductor manufacturing process specifying certain geometric and connectivity restrictions to ensure sufficient margins to account for variability in semiconductor manufacturing processes, so as to ensure that most of the parts work correctly.

Physical Verification
- drc all
- lvs all

Layout vs. Schematic is the class of electronic design automation verification software that determines whether a particular integrated circuit layout corresponds to the original schematic or circuit diagram of the design. LVS checking software recognizes the drawn shapes of the layout that represent the electrical components of the circuit, as well as the connections between them. The software then compares them with the schematic or circuit diagram. Typical errors encountered during LVS include: shorts, opens, component mismatches, missing components, property errors.

Calibre [calibre]

- package stream_out

Instantiates top-level package, inserts an instance of the final core cell into the package, places point-to-point wires in the design to represent bond-wires.

Design Compiler [dc_shell-t]

RTL Synthesis

RTL synthesis solution that performs advanced arithmetic optimisation, critical path synthesis, register retiming etc. It enables a developer to optimise a design for timing, area, power and test.

Power Compiler

Power Optimisation & Analysis

Power Compiler performs both RTL and gate-level power optimisation and gate-level power analysis. By applying Power Compiler's various power reduction techniques, including clock-gating, operand isolation, multivoltage leakage power optimization, and gate-level power optimization, you can achieve power savings, and area and timing optimisation in the front-end synthesis domain.

JupiterXT [JupiterXT]

SoC Hierarchical Design Planning

JupiterXT helps to partition the logical netlist into the best physical hierarchy for optimised synthesis and physical implementation.

Astro [Astro]

Physical Optimisation, Placement and Routing Solution for SoC Designs

Numerous technology-dependent steps are required to complete a complex, ultra-deep-submicron integrated circuit (IC) design. Logic and interconnect delays must be analysed and minimised. Physical effects such as signal crosstalk, power density, and supply voltage drop must be handled. Ideal clocks can no longer be assumed, and clock skew must be minimized. Physical effects are critical because changes to one may seriously impact the optimization of others.

The Astro product is an advanced physical design system for optimisation, placement and routing, using a specialised architecture that concurrently accounts for physical effects while optimizing the resulting design.

StarXtract [StarXtract]

Parasitic Extraction

With shrinking process technologies, increasing die size and clock frequency, interconnect parasitic effects have begun to manifest themselves in signal delay and noise. Consequently, interconnects now play an important role in the design flow. Today, IC design is interconnect-limited and the design flow is interconnect-driven. Star-RCXT is a parasitic extraction tool that models advanced process effects and has the capacity to handle large designs with tens of millions of transistors and cells.

PrimeTime STA [pt_shell]

Static Timing Analysis

Timing analysis solution for gate-level designs featuring comprehensive analysis including setup/hold/recovery, parasitic or SDF delay annotations and many more (see Synopsis product data sheet).

Calibre [calibre]

Physical Verification

Mentor's Calibre tool is used for layout verification and design rule checking.

EnCore - Calton Chip Layout

RTL to Gates Synthesis · Floorplanning · Configuration · Start · IP Libraries · RTL Database · Vendor Libraries · Design Rule Checking · GDS II OUT · RTL to Placed Gates Synthesis · EDA Database [Synopsis Milkyway DB] · Layout vs. Schematic · GDS II · IC Layout · Timing Analysis · Parasitic Extraction · Tape-out

Tape-out